

IMPROVING PREDICTIVE ACCURACY IN VLSI CIRCUIT DESIGN WITH SYNTHETIC DATA GENERATION

Khetarpal, Vidisha

Guru Tegh Bahadur Institute of Technology, GGSIPU, New Delhi

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ABSTRACT

An essential component of promoting innovation and dependability in contemporary electronic systems is the pursuit of improved prediction accuracy in the field of very large-scale integration (VLSI) circuit design. However, the problem of inadequate data frequently arises in the traditional design routes, making it difficult to achieve the appropriate level of precision. To improve the accuracy of future machine learning models in activities like performance evaluation, design, and testing—where training data is typically known to be very limited—this work explores the use of diffusion models to generate false data for electrical circuits. To support our suggested diffusion model, we conduct simulations in the HSPICE design environment using 22nm CMOS technology nodes to get real-world training data that is typical of the situation. Our findings show that data generated artificially via diffusion model closely resembles genuine data. We confirm the accuracy of the produced data and show that data augmentation is definitely useful for digital circuit VLSI design prediction analysis.

Keywords: Diffusion model, Digital circuits, Data, Accuracy, Error

INTRODUCTION

A progressive reduction in transistor size is occurring year after year in Very Large-Scale Integration (VLSI) circuits and systems as a result of the development of semiconductor

technology, which is in accordance with Moore's law. Increasing the number of transistors that can be contained into a compact silicon region is the driving force behind this ongoing effort to reduce the size of the features. In order to accomplish the ultimate objective of boosting the computing capabilities of consumer electronic devices, not only need the sizes of transistors be reduced, but the technology that connects them should also improve in a manner that is commensurate with.

There are millions or billions of semiconductors that are joined together on a single chip using the VLSI architecture, which is the most prevalent method of building coordinated circuits. The development of cutting-edge electronic devices that power our modern world, such as mobile phones, semiconductors, and Internet of Things devices, is made possible by the ability to configure VLSI. When technology becomes more complex and smaller, VLSI configuration confronts a number of challenges but also opens up new opportunities.

The intricacy of the VLSI arrangement is one of the major challenges that it presented. In order to fulfill the requirements for execution, power, and region, VLSI setup requires the management of intricate architectures, information pathways, memory ordering, and interconnects. An increase in the number of semiconductors that are packed onto a chip result in a significant increase in the complexity of designs. This provides a number of challenges for the planners, including the management of the plan sequence, the division of the plan into many modules, the simplification of the jobs involving logic and figure crunching, and the assurance that the plan is accurate and comprehensive. In addition, the complexity of the VLSI configuration also contributes to the complexity of the verification process. Verification refers to the task of auditing the usefulness, execution, and dependability of the plan at several levels of reflection, ranging from the reasoning to the framework. The process of confirmation is a laborious and time-consuming endeavor that requires the utilization of contemporary instruments and methods of verification, such as appropriate procedures, simulation, imitation, and prototyping. Check is furthermore vital for guaranteeing the quality and security of the outcome, specifically for applications that involve human lives, like clinical gadgets and independent automobiles.

The power of the board is an additional evaluation that is crucial for the VLSI configuration. The setup of a VLSI necessitates balancing execution with energy productivity and applying several processes, including as power gating, voltage scaling, and clock gating, in order to significantly increase power consumption. For the purpose of reducing the intensity dispersion

and further improving the battery duration of electronic devices, power the executives is an important factor. Nevertheless, the process of powering the board also poses new challenges for the planners. These challenges include the management of the sacrifices that must be made between performance and power, the management of the various types of power, and the ensuring of the steady quality and safety of the power supply. Furthermore, the power of the board also has an effect on the real plan issues, which are the difficulties of installing and directing a large number of components on a chip while simultaneously satisfying the criteria for timing, power, and environment. An actual plan is a complex project that necessitates the streamlining of floor planning, the utilization of advanced calculations for scenario and steering, and the resolution of concerns such as clog and sign honesty in order to achieve a plan that is truly formidable.

REVIEW OF LITERATURE

Vellingiri, Govindaraj & B, Arunadevi. (2021) Machine learning (ML) algorithms are currently garnering a great deal of attention in the majority of engineering applications. This is due to the fact that they are capable of modeling complicated systems by making use of past data. employing an approach that is based on passive machine learning, it is hypothesized that power estimation for CMOS VLSI circuits may be accomplished by employing a variety of circuit properties. The approach that has been developed makes use of the supervised learning method, which offers a quick and precise assessment of power without compromising the precision of the system.

A relatively recent development is the estimate of power using the random forest technique. In order to obtain an accurate prediction of the power of CMOS VLSI circuits, the random forest model is utilized. This model is then improved and tweaked through the utilization of the Mult objective NSGA-II algorithm. It can be deduced from the findings of the experiment that the testing error ranges from 1.4% to 6.8%, and the Mean Square Error in the random forest technique is $1.46e-06$ when compared to the BPNN method. Random Forest has been shown to be the most effective method for power estimate of CMOS VLSI circuits, with a high coefficient of determination of 0.99938 and a low Root Mean Square Error (RMSE) of 0.000116. This has been demonstrated by statistical estimating techniques such as the coefficient of determination (R) and Root Mean Square Error (RMSE).

Gaber, Lamya et al., (2020) The verification approaches have been significantly impacted by the recent exponential growth in complexity of digital VLSI circuits. The use of CAD has been

crucial to the development of methods for digital VLSI circuit verification and debugging. The increasing complexity of VLSI circuits has made existing methods increasingly reliant on specialized test patterns, the number of which has grown in recent years. The second issue is the long running time caused by the big injection circuit sizes and the high number of SAT solver calls. There are three main objectives that come into play here. Firstly, we want to reduce reliance on any one test pattern by gradually creating smaller test patterns that match the design mistakes that need fixing. Secondly, to correct errors more efficiently by reducing the size of the in-circuit mutation circuit. Virtually large-scale integrated circuits (VLSIs) with many inputs and outputs can now benefit from parallel distribution of test patterns. Several digital VLSI circuits from ISCAS'85 may have their design faults fixed quickly and accurately using the suggested incremental correction technique, according to the experimental results. Using the ISCAS'85 benchmarks, the suggested auto-correction system achieves a performance advantage of about 4.8x over the most recent approaches in existence. A speedup of around 1.2x compared to state-of-the-art approaches is achieved by creating new compact test patterns through the parallel distribution of test patterns on digital VLSI circuits.

Surwadkar, Tushar et al., (2019) Many novel digital and analog circuit designs have made use of FinFETs. While raising the channel doping density and aggressively scaling down the gate-oxide thickness are not necessary for successful control of the short-channel effects, the two gates for FinFETs do just that. Multiple threshold voltages can be readily provided by the independent biasing of DG devices. It may also be used to implement logic functions with fewer transistors. This project aims to investigate several logic design styles for FinFETs, such as SG, IG, LP, and IG/LP, and determine the optimal mode based on power consumption while studying their implications for low-power design. Half or more of the power used by CMOS circuits might be attributable to leakage power, according to estimates. Given that leakage power consumption continues to account for a significant portion of total power consumption, we investigate how to effectively address this issue by utilizing a mix of circuit design strategies and optimization at the logic level. The article delves into the topic of digital CMOS design and IDDG-FETs, specifically examining the use of independent-gate FinFETs.

Alawieh, Mohamed Baker et al., (2019) Design for manufacturability (DFM) is growing in importance and difficulty as integrated circuit technologies continue to be scaled down. Moreover, a new paradigm in computing has emerged because to advancements in machine learning, which may find useful applications in the field of very large-scale integration (VLSI) manufacturing. Among the most intriguing concepts in modern machine learning, generative

learning in particular has proven effective in many different contexts. Using generative learning for very large-scale integration (VLSI) industrial optimization and simulation, this paper compiles current findings. In particular, we take a look at how generative learning's distinctive properties have been used to boost DFM efficiency in a way that has never been seen before, opening the door to a fresh data-driven DFM strategy. The most recent approaches are detailed, and problems and possibilities are addressed.

Wang, Hai et al., (2015) Being mindful of temperature Nowadays, modern many-core and three-dimensional stacking architecture rely on very large-scale integration (VLSI) circuit design. The memory-and time-intensive thermal modeling and analysis is a major stumbling block in the design cycle. In this paper, we go over the module based thermal modeling approach, which involves breaking the chip into smaller parts and then putting together the reduced models of those parts to form the thermal model. In order to reduce the inaccuracy at the module borders, an accuracy enhancement framework is provided. Thermal analysis for very large-scale integration circuit design is facilitated by the suggested method, as demonstrated by experiments on multi-core microprocessors.

Perri, Stefania et al., (2010) In this research, VLSI circuits for Multiplication-Free Weighted SAD-based Variable Block-Size Motion Estimation are shown. By comparing it to current SAD-based circuits, we can see that we can obtain greater accuracy without sacrificing speed performance, but that our resource requirements can grow substantially. A power consumption of less than 100 $\mu\text{W}/\text{MHz}$ and an operating frequency more than 1 GHz were achieved by employing a 90 nm 1 V CMOS technology.

EXPERIMENTAL SETUP

When training Diffusion Denoising Probabilistic models, we make use of Python 3.8.16 and Google Colab. In addition, Tensorflow-2.9.2 and Keras-2.9.0 are utilized in our implementation. Every dataset undergoes a diffusion model development procedure that includes both forward and reverse circuit data processing. We move linearly from 0.001 to 0.02 for the forward process, adopting a variance of β_t . By utilizing an encoder-decoder design that incorporates continuous batch normalization, the inverse operation may be accomplished. Leaky ReLu activation is used by the model. While the forward process adds noise to the training data, turning it into pure noise, the reverse process learns to de-noise the data and forecast its original distribution. To create the synthetic data, the diffusion model must first be

trained. Then, the needed sample is obtained by sampling from a pure random noise and applying the trained reverse diffusion model.

RESULTS AND DISCUSSION

To obtain an accurate picture of performance, we compare the model's and the simulator's output feature values. Discovering the ideal layer count is the first step in the hyper-parameter search. Table 1 shows how well the model performs with different numbers of hidden layers. With 17 characteristics in the NOT gate dataset, a five-layer design is shown to be the best option. This design is likewise applicable to datasets with up to nineteen characteristics. A six-layered design was shown to optimally increase the learning capacity for datasets with 21 characteristics. Various learning rates will be the focus of our next investigation. A learning rate close to 0.0005 guarantees consistently low percentage mistakes across all features, as seen in Figure 1. A low number of mistakes is guaranteed across all features with a learning rate of 0.0005.

Table 1: Comparison of performance of models with different layers across all features

No. of layers	Avg. of MAPE (%)
6 hidden layers	12.8
5 hidden layers	3.49
4 hidden layers	10.3

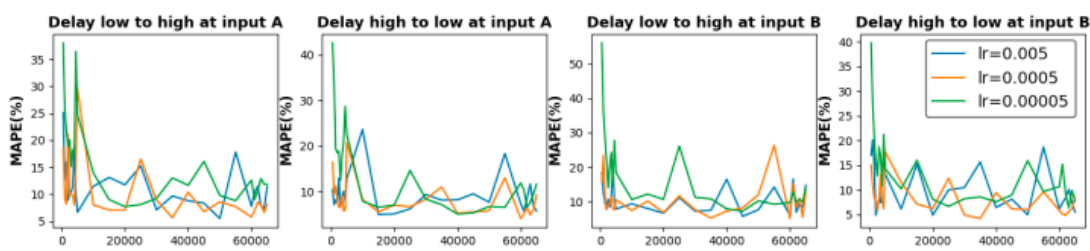


Figure 1: Performance of model with different learning rates w.r.t. HSPICE for delay in AND gate dataset

One may observe that all datasets achieve low MAPE (mean absolute percentage errors) by looking at Table 2, which displays the MAPE for all datasets.

Table 2: Percentage error obtained for different digital circuit datasets

Delay dataset	Mean Absolute Percentage Error					
	delay lh node a	delay hl node a	delay lh node b	delay hl node b	delay lh node c	delay hl node c
NOT gate	3.9	3.12	-	-	-	-
Two input NAND gate	4.41	6.3	4.54	7.52	-	-
Two input AND gate	5.76	4.12	5.13	5.84	-	-
Two input NOR gate	5.14	2.52	3.92	6.05	-	-
Two input OR gate	3.77	3.5	5.57	4.42	-	-
Two input XOR gate	0.34	3.44	4.04	2.94	-	-
Three input AND-OR circuit	7.96	4.83	4.74	8.33	4.3	8.55
FULL ADDER	2.85	2.85	3.62	5.93	2.15	4.42
2:1 MULTIPLEXER	3.81	3.27	2.91	5.53	3.68	4.03
Three input NAND gate	7.73	4.66	6.15	5.404	7.37	3.26
Three input AND gate	4.04	4.64	5.33	2.92	3.91	3.02
Three input NOR gate	4.57	5.007	5.11	6.46	3.74	5.13

Here, the error is calculated with respect to the HSPICE.

CONCLUSION

There is a revolutionary approach to improve the prediction accuracy of VLSI circuit design through the use of synthetic data generating techniques. The use of synthetic data generation has the potential to trigger a paradigm change in electronic design automation, leading the area of very large-scale integration circuit design to unprecedented levels of creativity and dependability. When it comes to pushing the boundaries of electronic systems, synthetic data

is a game-changer. It allows designers to imagine a future where accuracy and creativity meet, redefining what is possible.

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